AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A system for evaluating simulators using a circuit design comprising:

a processor;

a reference simulator configured to generate golden data by executing a first simulation image using the processor, wherein the first simulation image is compiled from a first implementation of the circuit design;

a test simulator configured to generate test data by executing a second simulation image, wherein the second simulation image is compiled from a second implementation of the circuit design; and

a comparator configured to select a portion of the test data, use a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test data, and generate a comparison result by comparing the portion of the golden data to the portion of the test data before the execution of the second simulation image on the test simulator has completed,

wherein the plurality of mapping rules map an internal hierarchy of the first implementation to an internal hierarchy of the second implementation, [[and]]

wherein the comparison result is used to debug the test simulator by correcting and displaying an error detected in the comparison result, and

wherein the reference simulator executes the first simulation image in lockstep with execution of the second simulation image.

2. (Previously Presented) The system of claim 1 further comprising:

a golden data repository storing the golden data.

3. (Original) The system of claim 1, wherein comparing the portion of the golden data to the portion of the test data occurs dynamically.

4. (Original) The system of claim 3 further comprising:
a buffer to store the golden data.

5. (Original) The system of claim 4, wherein the comparator is configured to wait to compare the portion of the golden data to the portion of the test data until after the golden data is stored in the buffer.

6. – 7. (Canceled)

8. (Previously Presented) The system of claim 1, wherein the mapping rule is obtained while the test simulator is halted.

9. – 10. (Canceled)

11. (Currently Amended) A method of evaluating a test simulator using a circuit design comprising:
executing a first simulation image on a reference simulator to obtain golden data, wherein the first simulation image is obtained by compiling a first implementation of the circuit design;
executing a second simulation image on the test simulator to obtain test data, wherein the second simulation image is obtained by compiling a second implementation of the circuit design;
selecting a portion of the test data;
using a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test data;
comparing the portion of the golden data to the portion of the test data to obtain a comparison result,
wherein the plurality of mapping rules map an internal hierarchy of the first implementation to an internal hierarchy of the second implementation; and
debugging the test simulator by correcting and displaying an error detected in the comparison result.

wherein executing the first simulation image on the reference simulator is performed in lockstep with executing the second simulation image.

12. – 14. (Canceled)

15. (Original) The method of claim 11 further comprising:
storing the golden data in a golden data repository.

16. – 17. (Canceled)

18. (Original) The method of claim 11, wherein the step of comparing the selected golden data to the selected test data waits on storing the golden data in a buffer.

19. (Previously Presented) The method of claim 11, wherein the step of selecting the portion of the test data is performed dynamically.

20. – 21. (Canceled)

22. (Previously Presented) The method of claim 11, wherein the step of executing the second simulation image is halted to obtain the mapping rule.

23. – 24. (Canceled)

25. (Currently Amended) A computer system for evaluating a test simulator using a circuit design comprising:
a processor;
a memory;
a storage device; and
software instructions stored in the memory for enabling the computer system to:
execute a first simulation image on a reference simulator to obtain golden data, wherein the first simulation image is obtained by compiling a first implementation of the circuit design;

execute a second simulation image on the test simulator to obtain test data, wherein the second simulation image is obtained by compiling a second implementation of the circuit design;

select a portion of the test data;

use a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test data; [[and]]

compare the portion of the golden data to the portion of the test data to obtain a comparison result,

wherein the plurality of mapping rules map an internal hierarchy of the first implementation to an internal hierarchy of the second implementation;

and

debug the test simulator by correcting and displaying an error detected in the comparison result,

wherein the reference simulator executes the first simulation image in lockstep with execution of the second simulation image.

26. – 32. (Canceled)

33. (Previously Presented) The system of claim 1, wherein the portion of the test data is generated after the golden data is generated.

34. – 35. (Canceled)

36. (Previously Presented) The method of claim 11, wherein the portion of the test data is generated after the golden data is generated.

37. – 38. (Canceled)

39. (Currently Amended) The computer system of claim [[25]] 23, wherein the portion of the test data is generated after the golden data is generated.

40. (Currently Amended) The method of claim 11,

wherein [[the]] a user data is altered while executing the second simulation image, and wherein the user data includes data that is used to evaluate the test simulator.

41. (Previously Presented) The method of claim 11, wherein the test simulator is debugged while executing the second simulation image.

42. (Previously Presented) The method of claim 11, wherein the comparison result is displayed while executing the second simulation image.